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04/04/05

PATENT APPLICATION

ATTORNEY DOCKET NO. 10004546-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Brian W. Hughes et al.

Confirmation No.: 7471

Application No.: 09/842,435

Examiner: J. D. Torres

Filing Date: April 25, 2001

Group Art Unit: 2133

Title: SYSTEM AND METHOD FOR MEMORY SEGMENT RELOCATION

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **02/01/2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United State Postal Service as Express Mail, Label No. EVEV482744410USUS in an envelope addressed to: Appeal Brief - Patents, Commissioner for Patents, Alexandria, VA 22313. Date of Deposit: April 1, 2005

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Number of pages:

Typed Name: Elise Perkins

Signature: Elise Perkins

Respectfully submitted,

Brian W. Hughes et al.

By _____

Michael A. Papalas

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Docket No.: 10004546-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Brian W. Hughes et al.

Application No.: 09/842,435 | Confirmation No.: 7471

Filed: April 25, 2001 | Art Unit: 2133

For: SYSTEM AND METHOD FOR MEMORY SEGMENT RELOCATION | Examiner: J. D. Torres

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on February 1, 2005, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II.	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument
VIII.	Claims
IX.	Evidence
X.	Related Proceedings
Appendix A	Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principle place of business in Houston, Texas.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 12 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: 1-10
2. Claims withdrawn from consideration but not canceled: 11-17
3. Claims pending: 18-29
4. Claims allowed: 0
5. Claims rejected: 18-29

C. Claims On Appeal

The claims on appeal are claims 18-29.

IV. STATUS OF AMENDMENTS

Appellant filed a Response After Final Rejection on December 6, 2004 which did not amend the claims. The Examiner responded to the Response After Final Rejection in an Advisory Action mailed January 3, 2005. In the Advisory Action, the Examiner indicated that the Response After Final Rejection did not place the application in condition for allowance.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to claims 18 and 19, the subject matter is a method for preserving an operation of a memory segment (100, Figure 1) that includes evaluating elements (203, Figure 2) of the memory segment in row fast order. Specification, page 8, lines 3-10 and page 5, lines 10-15. The method also includes identifying faulty ones (204, Figure 2) of the evaluated elements and determining a number of the identified faulty ones (205, Figure 2) of the evaluated elements in each of a plurality of subsets of the memory elements. Specification, page 8, lines 8-19. The method further includes comparing the determined number to a fault threshold value (210, Figure 2) and declaring a failure condition for the memory segment (213, Figure 2) if the determined number is greater than or equal to the fault threshold value for any one subset of the memory segment. Specification, page 8 line through page 9, line 2. The method also includes physically remapping the memory segment in response to the declared failure condition (214, Figure 2). Specification, page 10, line 26 through page 11 line 15.

Claim 20 defines a method for preserving an operation of a memory segment (100, Figure 1) that includes storing evaluation data in the memory segment and comparing the stored evaluation data to expected data for the elements of the memory segment. Specification, page 7, lines 1-15. The method also includes incrementing a failure counter (205, Figure 2) upon detection of a faulty element in the step of identifying. Specification, page 8, lines 6-10.

According to claims 21-25 and 27-28 , the subject matter is a method of evaluating a reliability of a memory segment (100, Figure 1) that includes successively scanning (203, Figure 2) each of a plurality of subsets of the memory segment, wherein each subset comprises at least two linear arrays of elements. Specification, page 8, lines 3-10 and page 6, lines 6-18. The method also includes re-mapping the memory segment (214, Figure 2) when a number of malfunctioning elements in any one subset is greater than or equal to a threshold number. Specification, page 10, lines 26 through page 9, line 15.

Claims 26 and 29 define a method of evaluating a reliability of a memory segment that includes successively scanning each of a plurality of subsets of the memory segment, wherein each subset comprises at least two linear arrays. Specification, page 8, lines 3-10 and page 6, lines 6-18. The method also includes avoiding recording a total number of the counted malfunctioning elements in the memory segment. Specification, page 9, line 21

through page 10, line 24. The method further includes resetting a count of malfunctioning elements after the analyzing step. Specification, page 9, line 21 through page 10, line 24.

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

A. First Ground of Rejection

Claims 18, 19, and 21-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 4,939,694 to Eaton et al. (hereinafter "Eaton") in view of U.S. Patent Number 4,460,997 to Harns (hereinafter "Harns").

B. Second Ground of Rejection

Claims 20 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eaton and Harns.

VII. ARGUMENT

A. Claims 18 and 19

With respect to claims 18 and 19, claim 18 defines a method that includes determining a number of said identified faulty ones of said evaluated elements in each plurality of subsets of said memory segments and physically re-mapping said memory segment in response to said declared failure condition. The Examiner does not dispute that Eaton discloses a memory system that is operable to logically remap defective memory locations to replacement memory locations using substitute memory table 3-11. (column 5, lines 16-19). The substitute memory table of Eaton can either be a look-up table for all memory locations, or a content addressable memory to look up only replaced memory locations. (column 5, lines 20-40 and column 7, lines 21-28). In either case, Eaton's only disclosed means of replacing defective memory locations requires a mapping function in some type of memory, meaning that Eaton logically remaps defective memory cells, in contrast to the physical re-mapping of claim 18. Harns is not relied upon as teaching the remapping of defective memory locations.

In the Advisory Action dated January 3, 2005, the Examiner states:

> Any time a logical memory location is remapped so is the physical memory location corresponding to the logical and physical memory locations. The Examiner asserts that if a logical memory location is found faulty, then the physical memory location corresponding to the logical memory location is faulty; hence remapping of the logical memory location corresponding to the physical memory location allows the logical memory location corresponding to the physical memory location to be remapped to a replacement logical memory location corresponding to the replacement physical memory location. What good would it do to remap the logical memory location and not the physical memory location corresponding to the logical memory location since it is the physical memory location that is faulty? A one to one mapping between physical location and logical location ensures that the logical locations are substantially the physical locations as well.

Most importantly, the Examiner concludes: "Hence Eaton teaches remapping defective physical memory locations."

The present invention includes "physically re-mapping", which has very different implications than the Examiner's mischaracterization of "remapping defective physical memory locations." When a defective memory location is logically remapped the defective physical memory location still has the same physical address lines which can still be used to physically address the defective memory location. The same cannot be said for the "physical re-mapping" of the present invention.

The combination of Eaton and Harns does not teach or suggest each and every feature of claim 18 and claim 19 through its dependency from claim 18. Therefore, claim 18 is patentable over the rejection of record.

B. Claim 20

Claim 20, through its dependency on claim 18, defines a method that includes determining a number of said identified faulty ones of said evaluated elements in each plurality of subsets of said memory segments and physically re-mapping said memory segment in response to said declared failure condition. Claim 20 further requires incrementing a failure counter upon detection of a faulty memory element in the step of identifying. Again, the Examiner does not dispute that Eaton discloses a memory system that is operable to logically remap defective memory locations to replacement memory locations using substitute memory table 3-11. (column 5, lines 16-19). Eaton logically remaps

defective memory cells, in contrast to the physical re-mapping of claim 20, and Harns is not relied upon as showing the limitation.

Further, the Examiner admits that "Eaton and Harns do not explicitly teach the specific use of a failure counter." While Eaton maintains the number of defective symbols in each record as cited by the Examiner at column 7, lines 14-17, Eaton does not disclose incrementing a failure counter upon detection of a faulty element as set forth in claim 20.

For the reasons set forth above, the Combination of Eaton and Harns does not teach every element of claim 20, therefore claim 20 is patentable over the rejection of record.

C. Claims 21-25 and 27-28

Claim 21, and each of claims 22-25, and 27-28 through their dependency from claim 21, require successively scanning each of a plurality of subsets of said memory segment, wherein each said subsets comprises at least two linear arrays of elements. Claim 21 specifically states that each subset comprises at least two linear arrays of memory elements. The Office Action relies solely upon Eaton as discloses testing individual memory cells 3-5 on memory chips 3-1. (column 4, lines 41-47). Eaton replaces defective individual memory cells, when located, by logically remapping the addresses for the defective cells to replacement cells. (column 5, line 8-19). Easton does not disclose a plurality of subsets of said memory segment wherein each subset comprises at least two linear arrays of elements.

The Examiner has asserted that the 64 byte data records used by Eaton in his error correction code engine 3-3 corresponds to the subsets of claim 21. Appellant respectfully asserts that this is clearly in error. The error correction code engine of Eaton is a data integrity mechanism between the memory system and the data bus that provides data error checking when data is read from the memory. This data error checking mechanism corrects for bit errors in the 64 bytes before the data is placed on the bus. The data errors checked for by the error correction engine is distinct from the testing and replacement of defective memory cells 3-5 and corrects error that can occur by means other than defective memory. (column 67, line 61-column 6, line 16). The subsets of claim 21 are subsets of memory elements and are successively scanned in evaluating the of the memory segment itself. Further, Eaton does not disclose that the records associated with his error correction code engine are made up of at least two linear arrays of elements.

Thus Eaton in combination with Harns does not teach all of the limitations of the invention claimed in claim 21. Therefore, Appellant respectfully asserts that the above reasons claim 21, and claims 22-25 and 27-28, are patentable over the rejection of record.

D. Claims 26 and 29

Claims 26 and 29, through their dependency from 21, require successively scanning each of a plurality of subsets of said memory segment, wherein each said subsets comprises at least two linear arrays of elements.

Claim 26 further requires avoiding recording a total number of said counted malfunctioning elements in said memory segment. With respect to claim 26, the Examiner, in the final office action dated October 6, 2004 stated that there is no indication that a total number of defects are kept for the IC chips in the Eaton patent. First, the claim requires that it is the total number of said counted malfunctioning elements in said memory segment, not the IC chip as characterized by the Examiner. Further, this assertion is in direct contradiction to the Examiner's citation of column 7, lines 14-17 of Eaton which the Examiner states that the ECC engine 3-3 is used to determine the number of defects in the segment. The cited section requires that Eaton maintain the number of defective symbols in each record. Therefore Eaton does not show avoiding recording a total number of said malfunctioning elements as required by claim 26.

Claim 29 further requires resetting a count of malfunctioning elements after said analyzing step. The Examiner states, with respect to claim 29 that the count has to be only retained for analysis of a record and afterwards must be reset to evaluate a new record in Eaton. The Examiner provides no support for this statement. In fact Eaton could permanently maintain separately the number of defective symbols in each record as set out in column 7, lines 14-17.

As neither Eaton, nor Harns, show the limitations set forth in claims 26 and 29, claims 26 and 29 are patentable over the rejection of record.

E. Lack of Motivation

There is no motivation in Eaton or Harns to combine the means for reading data out of memory described in Harns with the memory system of Eaton. The Examiner has stated that one skilled in the art would be highly motivated to combine Eaton with Harns to provide a means for reading data out of memory in Eaton, and that it would have been obvious to modify Eaton with the teachings of Harns by including use of evaluating elements in row-fast order. Final Office Action dated October 6, 2004. The Examiner has further stated that reading data out of memory still has a definite benefit to the user. Advisory Action dated January 3, 2005.

Appellant respectfully asserts that the statements of the Examiner are merely conclusory statements of the results of the combination put forward by the Examiner. The statements do not offer any motivation or reasons that the means of reading memory in Harns would have been of any benefit to the memory system of Eaton.

The Examiner further states in the final office action that the proposed modification would have been obvious because one of ordinary skill in the art would have recognized that evaluation elements in row fast order would have provided the means for reading data out of memory. The conclusion of the examiner forms a circular argument with respect to the conclusory statements made previously. The examiner is arguing that one would be motivated to combine Eaton and Harns to provide a means for reading the memory of Harns, and that the modification would be obvious because it would have provided a means for reading the memory of Eaton.

In addition, Eaton already has a means for reading the memory being tested (column 4, line 48-57), there is no suggestion that a different means for reading the memory would be beneficial, and the Examiner has provided no reasoning, other that conclusory statements, that would show any benefit from using the means of reading memory in Harns with the memory system of Eaton.

It is well settled that the fact that references can be combined or modified is not sufficient to establish a prima facie case of obviousness, M.P.E.P. § 2143.01. As stated above, the language of the recited motivation is circular in nature, stating that is obvious to make the modification because the achieved result is obvious. In addition, the language used by the Examiner is also conclusory, merely a statement that the reference can be modified,

and does not state any desirability for making the modification, nor does the Examiner explain why one would add the means for reading the memory of Harns to Eaton as the addition would be duplicative to the existing means for reading memory used by Eaton. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990), as cited in M.P.E.P. § 2143.01. Thus, the motivation provided by the Examiner is improper, as the motivation must establish the desirability for making the modification.

For reasons described above, the Examiner's combination of Eaton with Harns is improper because there is no motivation in either reference to make the combination. As a result, Appellant respectfully assert that claims 18-29 are allowable over the rejections based on the combination of Eaton and Harns.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

The fee for the Appeal Brief is noted on the Transmittal Sheet. Additionally, at any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account No. 08-2025, under Order No. 10004546-1, from which the undersigned is authorized to draw.

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Date of Deposit: April 1, 2005

Typed Name: Elise Perkins

Signature: Elise Perkins

Respectfully submitted,

By: _____

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Reg. No. 40,381
Date: April 1, 2005
Telephone No. (214) 855-8186

APPENDIX A

18. A method for preserving an operation of a memory segment, the method comprising the steps of:

evaluating elements of said memory segment in row-fast order;

identifying faulty ones of said evaluated elements;

determining a number of said identified faulty ones of said evaluated elements in each of a plurality of subsets of said memory segment;

comparing said determined number to a fault threshold value;

declaring a failure condition for said memory segment if said determined number is greater than or equal to said fault threshold value for any one said subset of said memory segment; and

physically re-mapping said memory segment in response to said declared failure condition.

19. The method of claim 18 wherein said identifying step comprises the steps of:

storing evaluation data in said elements of said memory segment;

comparing said stored evaluation data to expected data for said elements of said memory segment; and

identifying elements for which said stored evaluation data does not match said expected data.

20. The method of claim 18 wherein said determining step comprises the step of:

incrementing a failure counter upon detection of a faulty element in said step of identifying.

21. A method of evaluating a reliability of a memory segment, the method comprising the steps of:

successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements; and

re-mapping said memory segment when a number of malfunctioning elements in any one subset is greater than or equal to a threshold number.

22. The method of claim 21 wherein each said linear array is a row of said memory segment.

23. The method of claim 21 wherein each said linear array is a column of said memory segment.

24. The method of claim 21 further comprising:

setting a flag indicating one of a pass condition and a fail condition for said memory segment when a number of malfunctioning elements in any one subset is greater than or equal to a threshold number.

25. The method of claim 24 further comprising the step of:

discarding a result of said scanning upon completing said step of setting said flag.

26. The method of claim 21 further comprising the step of:

avoiding recording a total number of said counted malfunctioning elements in said memory segment.

27. The method of claim 21 further comprising the steps of:

loading test data into said memory segment;

reading said loaded test data from said memory segment; and

comparing said read loaded test data to expected data for at least one element of said memory segment.

28. The method of claim 21 further comprising the step of:

determining said fault threshold based upon at least one characteristic of said memory segment.

29. The method of claim 21 further comprising the step of:

resetting a count of malfunctioning elements after said analyzing step.